International Journal of Research in Engineering Technology-– Volume 3 Issue 1, Nov – Dec 2017

RESEARCH ARTICLE OPEN ACCESS

Design and Simulation of two switch DC-DC Forward Converter for Solar Application by using PSIM Software

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Abstract:

An isolated dc-dc converter is termed as forward converter. This converter has output power ratings between 50W to 400W. Along with conventional forward converter we require a transformer for tertiary winding to subject its power switch to a high voltage at turn off position. This disadvantage is overcome in two switch forward converter. The converter equations, its design, its waveform all studied .At last we have experimental results to confirm the design in solar power applications.

Keywords **— Forward Converter, PSIM Simulation, Solar Power, Feedback Controller.**

INTRODUCTION

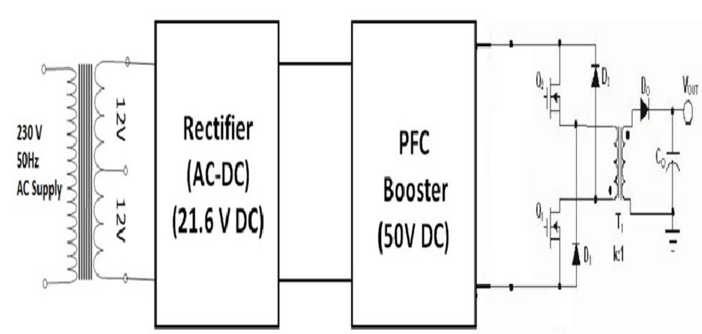
Two switch forward converter are almost used everywhere they are also believed to be the most reliable converter ever produced .They do not require snubber circuit for their operation. They have the tendency to operate multiple isolated output their operation is quiet simple .They fail to do zero voltage switching .They require two Mosfet as well as same amount of diodes for their operation to take place . Two switch forward converter to require an inductor for their operation [1].

The aim of this work is to make a Multiple Output Dc-Dc Converter on the basis of two switch forward converter topology. This Dc-Dc converter is developing to give multiple output power rails for usual requirement in industrial application. It has the battery supply that varies between 24v-36v. Along with necessary compensation circuits converter works in closed loop mode. By the use of control winding the loop feedback is closed. By making use of gate drive transformers input output isolation can be obtain.

The two switch forward converter topology has two mosfet switches one can get this ides from the name itself. Two switch forward converter works in two modes which are as follows in first mode Q1 and Q2 are turned on. It connects the input voltage source to the primary winding due to this both the windings start conducting together with the turning on of the switches [2].

When Q1 and Q2 are turned off. The magnetizing current flows through the forward biased diodes on the primary transformer and then back into the source.

Block Diagram



Steps for PFC Boost Converter

Input Power $p_{in} = \frac{p_{out}}{\eta}$

RMS Input current $I_{in(Rms)} = \frac{P_{in}}{V_{in(RMS)}}$

Maximum Input Current $I_{in(\max)} = \sqrt{2} \times I_{in(RMS)}$

According to IEC 1000 harmonic distortion specifications, the current ripple is (= 20 % of the I in(max)) considered. Therefore the current Δ*i* passing through inductor is to be,

$$I_L = 0.2 \times I_{in(\max)}$$

$$I_{in(avg)} = \frac{2 \times I_{in(\max)}}{\pi}$$

$$I_{out(\max)} = \frac{P_{out}}{V_{out(\max)}}$$

Duty Cycle D = $\frac{V_{out(\max)} - V_{in(\max)}}{V_{out(\max)}} \times 100$

Where; Pout = DC output power, Pin = AC input power, η = Input efficiency, Vin (rms) = AC input RMS current Iin(max) = AC input maximum current, Iin(avg)= Average AC input current, I_L = Inductor current [3].
Δ*i* = Inductor current ripple, Iout(max) = Maximum DC output current

The selection of inductor and the capacitor in the Boost topology plays a major role in the output response

$$L = \frac{V_{in(\min)} \times D}{F_{s/w} \times \Delta i}$$

Where; L = Inductance, s/w F = Switching Frequency, Vin (min) = Minimum input voltage,
D= Duty cycle
Here consider 5 % tolerance in output voltages so that the value of the output Capacitor is,

$$C_{out} = \frac{I_{out(\max)} \times D}{F_{s/w} \times \Delta V_{out}}$$

Where; ΔVout = Output Voltage ripple, Cout = Output capacitance [4].

Design of High Frequency Transformer

Secondary Output Power $p_o = (V_o + V_{rl} + V) \times I_o$

Where; rl V = Resistive Drop in the Inductor [≈ 10 % of o V d], V = Output Diode drop [≈ 1.5 V in worst case]

Area of Product $A_p = \frac{\sqrt{D_{\max}} \times P_o \times (1 + \frac{1}{\eta})}{K_W \times J \times B_m \times F_{s/w}}$

Where; K w = Window Utilization Factor [≈ 0.3 to 0.4],
B m = Max. Allowable flux density [≈ 0.2 T to 0.3T]
J = Current Density,
Ac = Area of core

Window Area $A_w = \frac{A_p}{A_c}$

Primary turns $N_1 = \frac{V_{i(\max)} \times D_{\min}}{A_c \times B_m \times F_{s/w}}$

Turns Ratio $n = \frac{V_o \times V_{rl} \times V_d}{V_{i(\min)} \times D_{\max}}$

Secondary turns $N_2 = n \times N_1$

Where; RMS Secondary Current $I_2 = I_o \times \sqrt{D_{\max}}$

RMS Secondary Current $I_1 = n \times I_2$

Primary Inductance $L_1 = \frac{\mu_o \times \mu_r \times A_c \times N_1^2}{I_m}$

Magnetizing Current $I_{mag} = \dfrac{D_{max} \times V_{i(min)}}{F_{s/w} \times L_1}$

Area of Primary Conductor $a_p = \dfrac{I_1}{J}$

Area of Secondary Conductor $a_s = \dfrac{I_2}{J}$

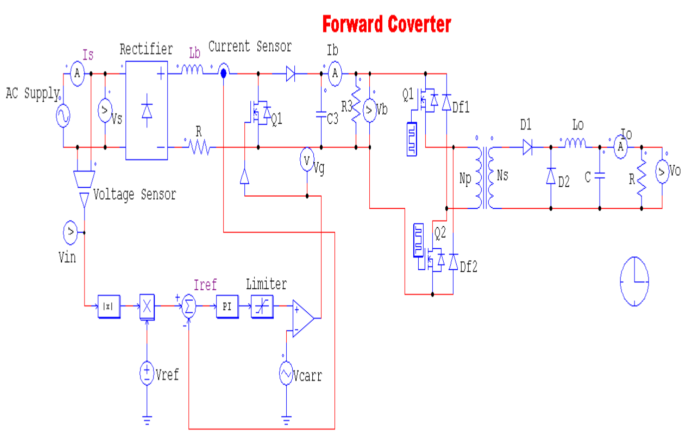
Design of Output Inductor

Output Inductance $L = \dfrac{V_0 \times (1 - D_{max})}{\Delta i \times F_{S/w}}$

Area of product $A_p = \dfrac{2E}{K_W \times K_C \times J \times B_m}$

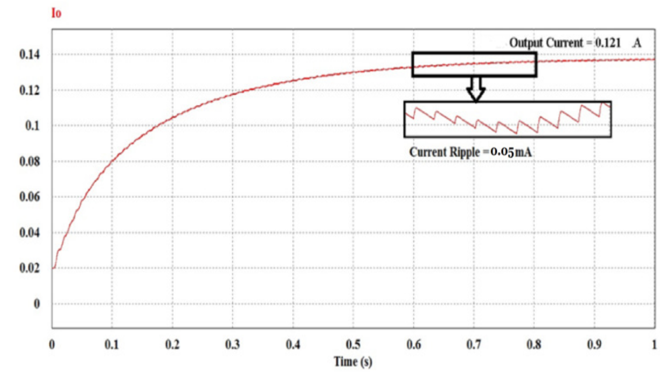
Where; E=Energy Dissipation in inductor

Simulation

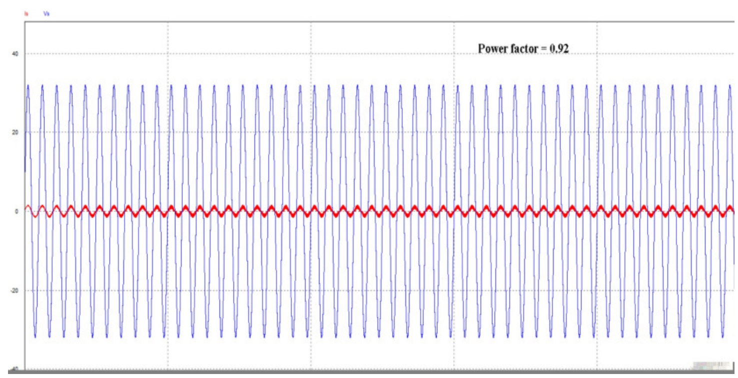


[5].

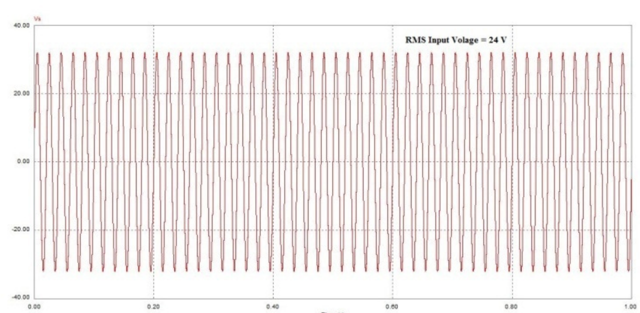
Current Ripple Waveform



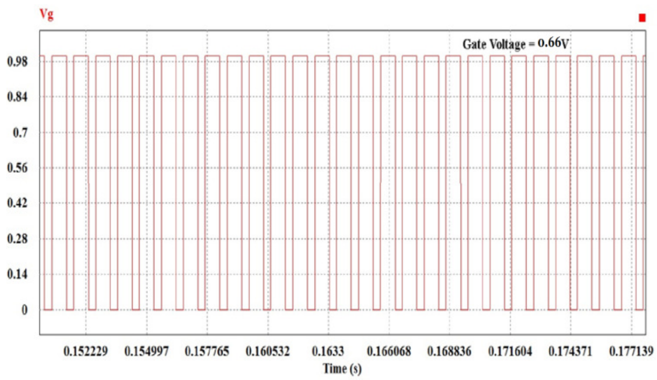
Power Factor Waveform



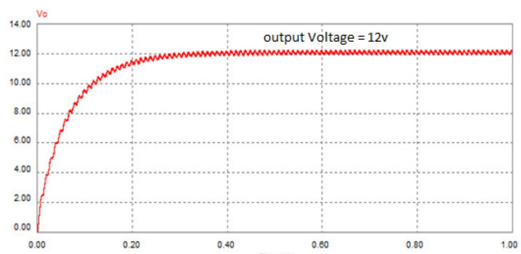
RMS Input Voltage Waveform



Gate Voltage Waveform



Output Voltage Waveform



Conclusion:

We can implement this project in solar power applications. By using this project the voltage stress can be reduced to a lower level and also power factor of the system as well as the efficiency can be improved to a benefiting level.

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